6. Claims

(1) A kind of manufacturing method for the non-volatile memory, including the following steps:

build a gate dielectric layer on a base, the gate dielectric layer contains at least two layers of different material layers;

at least one hetero element is planted on the top of the gate dielectric layer so as to increase the electronic trap density;

rebuild a new top material after removing the upmost layer of material, and build a gate electrode layer on the gate dielectric layer and form source / drain electrodes at the bases of both sides of the gate dielectric layer.

(2) A kind of manufacturing method for the non-volatile memory as the method in claim 1, where the gate dielectric layer is composed by three layers of materials, in turns from bottom to the top are a first oxide layer, a nitride layer and a second oxide layer.

(3) A kind of manufacturing method for the non-volatile memory as the method in claim 1, where the hetero elements used are any one within Germanium (Ge), Silicon (Si), Nitrogen (N_2), Oxygen (O_2), Nitrogen (N), Oxygen (O) separately or multiple mixture therefrom.

(4) A kind of manufacturing method for the non-volatile memory as the method in claim 1, where the hetero elements used are compounds of Germanium (Ge), Silicon (Si), Nitrogen , Oxygen (O).

(5) A kind of manufacturing method for the non-volatile memory, including the following steps:

build a gate dielectric layer on a base, the gate dielectric layer contains at least two layers of different material layers;

at least one hetero element is planted on the top of the gate dielectric layer so as to increase the electronic trap density, and

build a gate electrode layer on the gate dielectric layer and form source / drain electrodes at the bases of both sides of the gate dielectric layer.

(6) A kind of manufacturing method for the non-volatile memory as the method in claim 5, where the gate dielectric layer is composed by three layers of materials, in turns from bottom to the top are a first oxide layer, a nitride layer and a second oxide layer.

(7) A kind of manufacturing method for the non-volatile memory as the method in claim 5, where the hetero elements used are any one within Germanium (Ge), Silicon (Si), Nitrogen (N_2), Oxygen (O_2), Nitrogen (N), Oxygen (O) separately or multiple mixture therefrom.

(8) A kind of manufacturing method for the non-volatile memory as the method in claim 5, where the hetero elements used are compounds of Germanium (Ge), Silicon (Si), Nitrogen , Oxygen (O).

(9) A kind of manufacturing method for the non-volatile memory as the method in claim 5, where the gate dielectric layer is composed by two layers of materials, in turns from bottom to the top are an oxide layer and a charge storage layer.

(10) A kind of manufacturing method for the non-volatile memory as the method in claim 9, where the charge storage layer is chosed one between silicon nitride and aluminum oxide.

(11) A kind of non-volatile memory structure, including:

a base;

a gate dielectric layer on the base, the gate dielectric layer has at least one kind of hetero element to increase the electron trapping density;

a gate electrode layer on the top of the said gate dielectric layer;

and a source / drain electrodes at the base on both sides of the said gate dielectric layer.

(12) A kind of non-volatile memory structure, as the structure in claim 11, where the gate dielectric layer in turns from bottom to the top including a first oxide layer, a nitride layer and a second oxide layer.

(13) A kind of non-volatile memory structure, as the structure in claim 11, where the hetero elements used are any one within Germanium (Ge), Silicon (Si), Nitrogen (N_2), Oxygen (O_2), Nitrogen (N), Oxygen (O) separately or multiple mixture therefrom.

(14) A kind of non-volatile memory structure, as the structure in claim 11, where the hetero elements used are compounds of Germanium (Ge), Silicon (Si), Nitrogen (N), Oxygen (O).